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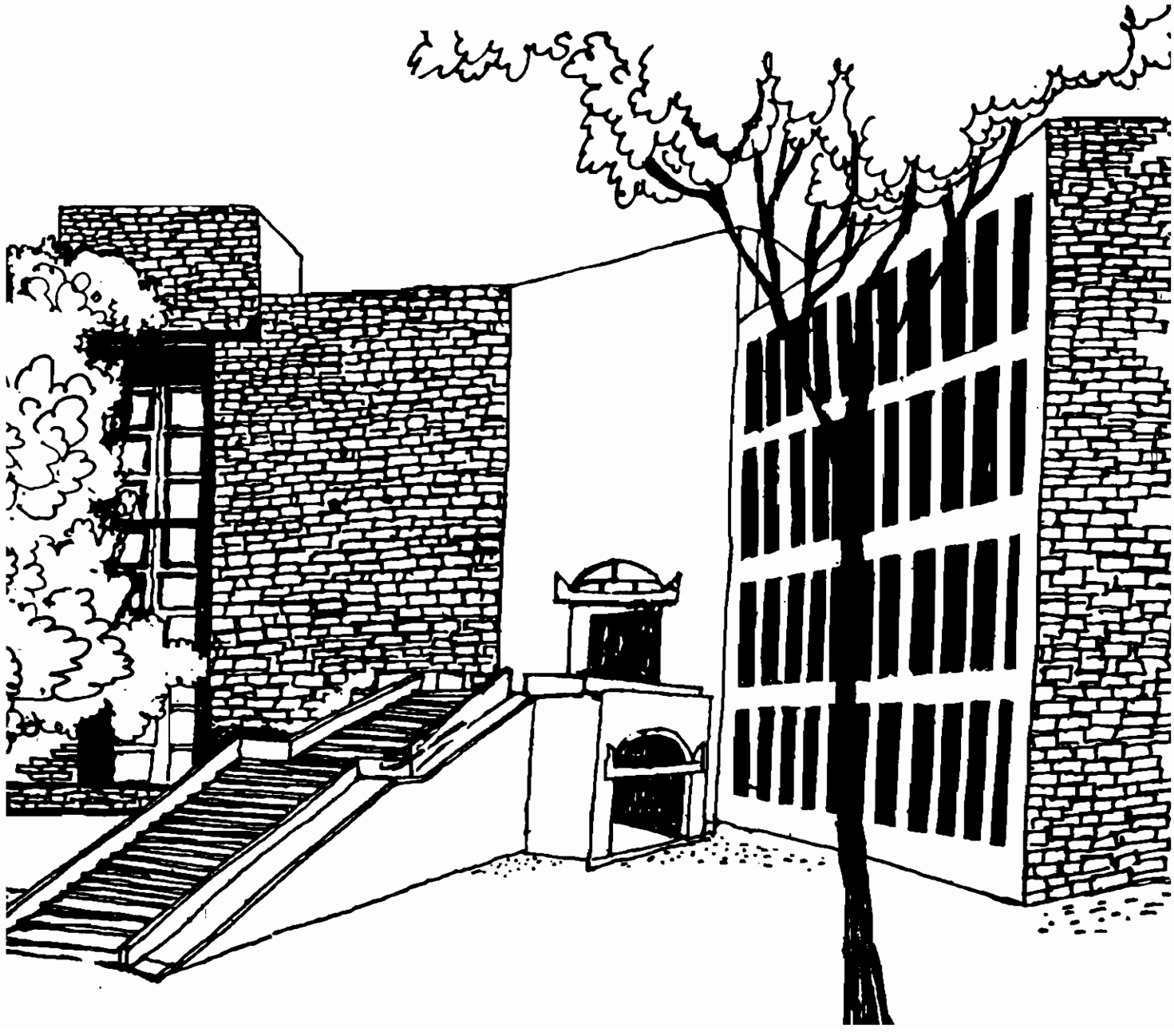

ORDER RELEASE AND PRODUCT MIX COORDINATION IN A COMPLEX PCB MANUFACTURING LINE WITH BATCH PROCESSORS

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Abstract

In this paper we study the role of order releases and product mix coordination in a complex manufacturing line with batch processors. We develop a planning methodology for synchronizing production in such manufacturing lines and discuss the decision making process in the context of a PCB production environment at Northern Telecom's Fiberworld Division. The planning methodology includes developing mathematical programming models for determining a configuration of batch processors, order releases to the shop floor, and daily loading decisions at the batch processors. The optimization models are linked to a simulation model of the shop which provides key statistics like lead time, work-in-process, utilization rates, etc. The objective is to reduce lead time for manufacturing different products in this environment while meeting the demand. We analyze the performance of such a line, study the efficacy of various types of shop floor synchronization policies, and establish the role of batch processors in managing such complex lines effectively. We exhibit how batch processors (which are bottleneck operations) could be scheduled effectively so as to incorporate the logical constraints that govern their operations and react to variabilities in the manufacturing line.

Key Words

Manufacturing Operations, Job Release Policy, Batch Processor, Machine Loading, Printed Circuit Board Manufacturing.

1 Introduction

In this paper we address a problem encountered in various industries where a batch processor is a part of a complex manufacturing line. A batch processor can process more than one unit of a product at a time (unlike a discrete processor which processes one unit at a time), and once a batch process begins it cannot be interrupted until the entire batch is processed. Such batch processors include burn-in ovens in a semiconductor packaging or a printed circuit board (PCB) manufacturing line, diffusion and oxidation stages in wafer fabrication and heat treatment facilities found in steel and ceramic industries, as well as various bath treatments in the chemical and metallurgical industries. The processing time on a batch processor is, usually, the largest of any station in such a manufacturing line. A batch processor is usually subject to constraints that limit the batch size and/or composition. In the simplest case, a maximum number of units is allowed in the batch processor at any time, whereas in other situations, there may be constraints on the total space available or on the mix of items that is allowed in the batch.

The generic system under study comprises two stages - the first stage consists of several (serial or parallel) discrete processors while the second stage consists of one or more parallel (although not necessarily identical) batch processing machines. The batch processor has certain restrictions on the mix of products that can be processed in a batch. Monthly demand is provided for each product and the objective is to reduce the lead time for manufacturing these products. Units that are released into the line are first processed by the first stage but have to wait in front of the batch processor until a "logical" batch (i.e., one that satisfies the mix constraints of the processor) has accumulated and may thus be processed. It can be appreciated that large release batches, or stringent mix constraints, can cause work-in-process inventory (WIP) to build up before the batch processor. As a result, any order release policy should aim at coordinating the product mix to meet the mix requirements of the batch processor. In other words, the batch processor should "pull" its requirement from the preceding stage in the manufacturing line.

In this article, we develop a planning methodology that can be used for the coordi-

nation of production in a manufacturing line that includes batch processors. We describe the objectives of the problem and the decision making process in the context of a complex PCB manufacturing line at Northern Telecom's (NT) Fiberworld Division in St. Laurent, Quebec. The two stages in this PCB manufacturing operations are as follows: the first stage consists of several operations such as component mounting, insertion and testing of individual PCB's, whereas the second stage is a burn-in operation that performs a final test on collections of PCBs forming fully functional systems. The goal of the project was to reduce the lead times on the shop floor. The current lead times, as observed in the plant, was about 15 days per PCB.

Much of the previous work related to multi-stage manufacturing is based on the study of a static shop, i.e., one where the effective processing time at a station for any part is known and fixed. Karmarkar [1987a, 1987b] has shown that the effective processing time at any station is a function of the lot size. As a result, the effect on congestion of the shop needs to be incorporated in choosing an order release policy, if we are to estimate lead times correctly. Most analytical results are derived for lines with very few stations and rarely in conjunction with batching type decisions on lines with setups (e.g., Awate and Sastry [1987] and Dallery and Gershwin [1991]).

From a different but related angle, queueing network theory has allowed the computation of WIP and lead times for a very limited set of release policies: for example, open queueing networks tackle the case where a release is directly triggered by the occurence of a demand, whereas closed networks can mimic a few other policies where an item completion triggers a new release. Karmarkar et al. [1985a] model job shops as an open network of queues and develop heuristics for determining lot sizes in a multi-machine environment. The reader is also referred to Buzacott and Yao [1986] and Hsu et al. [1993] for surveys of manufacturing applications of queueing models.

It is generally difficult to compute lead times analytically for complex, multi-product production lines, especially when logical constraints (such as the ones alluded to above) govern the operation of some of the stations in the line. This inability to use tractable analytical models for solving problems with complex structures has led to simulation oriented analy-

ses. Lin et al. [1987] and McDowell and Randhawa [1989] have developed simulation based decision support systems for analyzing PCB fabrication lines. Karmarkar et al. [1985b] have combined simulation with analytical models to examine the characteristics of a manufacturing cell at Eastman Kodak's Apparatus Division. Another recent paper that studies the role of WIP in serial lines using simulation is Conway et al. [1988]. Somcothers who have written on order release policies in the context of semiconductor manufacturing are Glassey and Resende [1988], Wein [1988], and Akella et al. [1992]. None of the above, however, model the more complex burn-in like operations.

The presence of the burn-in operation and the related constraints pose a new set of optimization problems in trying to manage the larger manufacturing line. The loading pattern of the burn-in ovens has a significant impact on the WIP and consequently on lead times. Any attempt to reduce lead times will have to synchronize the order release policies on the shop floor with the loading plans for the burn-in ovens. The interest in modelling batch processors is quite recent. Most papers on batch processing operations address the loading issues in isolation of the order release issue (e.g., Ikura and Gimple [1988], Glassey and Weng [1992], Fowler et al. [1992], Lee et al. [1992], Dobson and Nambimadom [1992], Chandru et al. [1993] and Uzsoy [1994].). They have considered a single batch operation with different types of contraints. Lee et al. [1992] and Dobson and Nambimadom [1992] acknowledge the necessity of integrating these models with those at other stations in the shop as it is not obvious that decisions from such isolated models will be valid in the context of a multi-stage manufacturing line. Ahmadi et al. [1992], Chandra and Gupta [1992] and Gurnani et al. [1992] are apparently the only papers which model batch and discrete processors together in the context of a multi-stage manufacturing line. Ahmadi et al. models a two machine system where one of the machines is a batch processor while the other is a discrete processor with no setups. They devise order release policies to minimize the makespan in the shop. Chandra and Gupta model batch processors in a semiconductor packaging line where processing times are constant for all parts and there is no variability in the production process. They establish the relationship between burn-in oven loading and lead times and illustrate the need to manage the WIP at the batch processor to minimize lead times. Gurnani et al. [1992]

use bulk queuing procedures for modeling a generic serial-batch system where the machines are subject to failures and design a control limit policy (i.e., wait until a defined length of the queue is built up) for batch loading. Only Chandra and Gupta [1992] address the requirements of multiple part production in this context.

In the following section we describe the problem in detail and discuss the product and the process structures. In section 3 we present the decision framework and describe a planning methodology as well as the models therein. Our approach incorporates optimization models within a simulation framework to evaluate various order release and loading policies. In section 4 we describe how our planning methodology is used to reduce the average lead time substantially on the shop floor. We illustrate the role of synchronization in reducing WIP and show how shop floor performance deteriorates when capacity of the batch processors is highly utilized. Section 5 provides the conclusion and points towards some issues that remain to be addressed.

2 Problem Description

Northern Telecom's Fiberworld Division produces various types of end products, which are transmission devices in NT's family of SONET based products (a proprietary technology), and sold to telecom companies and other industrial users. Transmission devices are digital multiplexing systems which essentially transmit digital signals over short/long distances.

The objective of this research is to determine a production plan that meets the monthly demand at a minimum lead time or equivalently to minimize the WIP while meeting the demand requirements. This would allow the firm to (a) reduce inventory build-up of on the shop floor and (b) produce closer to due dates. This is in congruence with the firm's desire to reduce dis-satisfaction of the customer due to delivery delays. In the following paragraphs we describe the manufacturing environment and discuss the issues under consideration.

Production Planning

Each transmission device comprises a set of printed circuit boards and other accessories as specified by a customer. Production on the shop floor is driven by firm orders of these transmission devices and for individual printed circuit boards, as well as forecast quantities for individual printed circuit boards. All the demands are translated into requirements for specific PCBs. The monthly production plans are determined in terms of these PCB requirements. Requirements are updated each month. For our study, we used the actual demand faced by the firm over a 11 month period. The total annual demand for all the PCBs was 44,462. The mean monthly total demand was 4042 and the standard deviation was 847. There was little or no inventory of finished products, since production was made to orders principally, and delivered to customers upon completion.

Product Structure

The end product is a collection of PCBs in a large bay and is called a *transmission device.* The average cost of a bay is $150,000. There are three types of transmission devices depending on the type of task required in the transmission and receipt of signals: OC-48, OC-12, and REGEN. Each device comprises a set of *sub-assemblies* (e.g., 7E02XX, 7E04XX, 8E03XX etc.). There are 38 different sub-assemblies. Each sub-assembly consists of one or more *printed circuit boards* (e.g., 7E0210, 7E0208, 7E0204 etc.). There are 60 different types of PCBs. Table 1 shows the product structure, e.g., one OC-12 comprises sub-assemblies 7E02XX, 7E08XX, etc. Sub-assembly 7E02XX is made up of PCBs 7E0210, 7E0208 etc. Note that some sub-assemblies such as 7E08XX comprise of a single PCB, i.e., 7E08AA. It is also possible that a PCB may be a part of more than one sub-assembly and that a sub-assembly can also be used in more than one product. Each printed circuit board is released into the line in the form of a *panel* of standard size. A panel may contain a single PCB, or several identical PCBs, depending on the physical size of the PCB (e.g. a certain panel contains 27 copies of the 7E0208 PCB). The standard size of panels facilitates the automation of material handling by rail conveyors.

A Guided Tour of the Production Line

The manufacturing line comprises four sections: the Automated Mounting & Insertion Section, the Manual Insertion and Assembly Section, the Testing Section, and the Burn-In Section (Figure 1). The first three sections comprise discrete processors. In the **Automated Mounting & Insertion Section**, circuitry is printed and solder paste is spread selectively on the PCB by a screen printer, and then the board is populated with components using surface mount technology as well as through-hole technology. All these can withstand wave soldering. Components of different types and shapes are either mounted on both sides of the PCB using "top side", "bottom side" machines , or inserted using "through hole" insertion machines. Some PCBs go through an additional set of operations (connector assembly, mold seal and modification before wave) before passing on to the next section. The **Manual Insertion and Assembly Section** consists of two segments: in the first segment, referred to as the Manual Insertion, first, additional components that can withstand wave soldering are inserted into the PCB which then passes through an automated "wave soldering" machine. Next, the remaining components, which cannot withstand wave soldering, are inserted on the PCB. In the second segment, individual PCBs are *depanneled* (broken apart into individual PCBs) and then a set of different PCBs (i.e., the "assembly set") are assembled into a sub-assembly at the Assembly stations. These operations are done manually. Up to the depanneling station, PCBs flow in a standard panel size. From this stage onwards, sub-assemblies are tested.

Two types of tests are performed in the **Testing Section**. The first test is called the "in-circuit" test which checks the integrity of the circuits. This test is performed at two locations: one dedicated to the 7E product line and the other to 8E product line. Each location comprises two parallel testing stations. Any "reject" is sent for trouble-shooting and repair before being re-tested. The first-pass yield at the in-circuit stations is between 30–60%. The second type of testing in this section is called the "functional test". Here the sub-assembly is tested as to whether it is performing its collective function. The functional test is performed at eight locations and each location may have more than one test station.

Each PCB type is allocated to a unique location and more than one type of PCB can be allocated to each location. Rejects, once again, go through trouble-shooting, repair, and re-test. The first-pass yield, here, ranges between 35–98%. The second-pass yield at both the tests is normally 100%.

The last section in the line, the **Burn-In Section**, comprises a number of batch processors, i.e., burn-in ovens. Each PCB is supposed to contribute to the functionality of the end product (as a whole) and that too in the field. This is tested (i.e., simulated) in the Burn-In ovens. Hence, the purpose of these ovens is twofold: first, it is to test whether the end product (i.e., a transmission device consisting of a set of assemblies) functions as a unit. The second purpose of the oven is to subject the end product to various temperature profiles while continuously testing its functions. The burn-in oven is the most challenging process in the entire line. There are two sizes of ovens: small and large. Currently, the manufacturing facility has four small and five large ovens. Ovens can only be loaded in specific combinations, or kits. A small oven can be loaded with any combination of 1 to 2 OC-48s and 0 to 2 REGENs. As a rule, REGEN cannot be tested alone. Each large oven can be wired into any of the following three configurations, each allowing different combinations of logical devices: either 1 to 8 OC-12s, or 1 to 2 OC-48s and 0 to 4 REGENs, or 1 to 4 OC-48s. It takes over eight hours to change the wiring configuration of a large oven. Finally, variations in the composition of a transmission device are allowed in the burn-in operation; these are summarized by a set of minimum and maximum numbers of sub-assemblies that are allowed in a particular device. A PCB that is tested as part of a given product may later on be delivered to a customer as part of another device.

Figure 1 is a representation of the complete line. However, not all PCBs go through all workstations. Some exit at locations which are shown in this figure. At each station except burn-in, PCBs are processed either in the form of a panel or in the form of a sub-assembly. However, in the oven, only *configurations* of devices can be tested. As a result, each time an oven is to be run, a decision has to be made regarding the configuration of the "logical" device (e.g., 4 units OC-48 or 2 units OC-48 etc.) that will be loaded in the oven. This "logical" end product is made out from the product mix available as WIP in the

Burn-in Section. Needless to mention, the "logical" end product that is being tested in the oven can be different from the end product demanded by a customer, or from the mix of separate sub-assemblies that may be in demand this month. To provide flexibility, there also exist **captive sub-assemblies** of different types that could be used to complete a "logical" mix. Such captives are used only for testing purposes, and are never shipped to customers. After going through burn-in a certain number of times, captives are scrapped. As PCBs are expensive, one aim of the research was to analyze the sensitivity of lead times to the number of available captive PCBs. After burn in, sub-assemblies are taken out of the oven, and then either mounted into bays according to customer demands for complete devices, or sent to warehouse as independent sub-assemblies/PCBs to satisfy demand for individual units from different customers. Table 2 gives the processing and setup times at different stations in the manufacturing line. Note that significant setups exist mainly at the screen printer and at the in-circuit test. The burn-in ovens have long process times and need to be carefully examined in developing any planning methodology.

3 The Decision Framework: Wiring, Order Release and Burn-In Plans

The decision framework shown in Figure 2 is closely modelled by the planning methodology shown in Figure 3 which we now describe: For the purpose of this study, the detailed operations of the shop are simulated by a GPSS/H program which computes the WIP levels, lead times, and other statistics of interest. The simulation requires as inputs: a monthly wiring plan (which determines which transmission devices may be loaded in each oven during that month), a daily order release plan (each day at 8:00 am it specifies the quantity and sequence of the different panels released in the simulated shop), and a daily burn-in plan (each day at 8:00 am it specifies which sub-assemblies to load in each burn-in oven during that day). In addition, a few decision rules are required at some intermediate work stations to specify batching and priority decisions.

For the purpose of this study, all capacities were taken as given, assuming that the line was balanced. This was confirmed by direct observation as well as by our results. Had this not been the case, our methodology would have identified locations with insufficient capacity.

The wiring plan ensures that the ovens are adequately setup to handle next month's demand. The daily release plan tries to ensure that the demand requirements are being met while trying to release a logical mix of PCBs that could eventually form a load in the ovens. If all the PCBs that were released over a one-day period arrive at the burn-in section also within one day (some days later), the release plan for those boards would automatically become the burn-in plan. However, because of unequal processing times and the occurrence of random events such as test failures and machine breakdowns, the sub-assemblies that are ready for burn-in test at the end of a day may not exactly match the release plan of some previous day. It is then important to re-design a burn-in plan, daily, based on the actually available mix of PCBs in the burn-in section and those that may soon be arriving there. Most often, the burn-in plan will be different from the release plan.

We now describe each of the three plans, the wiring, the release, and the burn-in plans in some detail, followed by several remarks concerning the other decisions at the intermediate stations. All three plans are modeled as integer programs which are solved using GAMS/LAMPS on a VAX 3100. The GPSS/H program dynamically calls GAMS at appropriate times.

3.1 The Wiring Plan

Each burn-in oven is wired to test a subset of three different devices: OC-12 only, OC-48 only, and OC-48+REGEN. Once a wiring is selected, the oven can only test the corresponding devices (however, the exact number of devices per oven is determined daily by the Burn-in plan). Since re-wiring ovens involves substantial loss of capacity and manpower, it is not effective or efficient to use re-wiring as a strategy to overcome the short term fluctuations in the mix of sub-assemblies available before burn-in. On the other hand, since the monthly

demand mix for the sub-asssemblies may vary considerably between two consecutive months, monthly re-wiring sometimes becomes desirable or even necessary to ensure that ovens are capable of testing all PCB types that are required in the coming month. The wiring decision is made at the beginning of each month and determines how many ovens will be wired using each of the three basic wirings. If more than one wiring option is feasible to satisfy the monthly demand, the plan chooses the one that requires the least number of ovens to be re-wired (as compared to the current wiring). It also assumes that the wiring process does not consume productive capacity though the time of engineers etc. is sought to be minimized. The model for determining the wiring plan is given below:

Indices:

i = index for PCB types.

m = index for wiring options.

Parameters:

M = number of wiring options ($M = 3$).

J = number of ovens available ($J = 9$).

$C(i,m)$ = maximum number of PCB i required for the wiring option m.

$D(i)$ = monthly demand for PCB i.

H = number of Burn-In cycles available in a month

= (22 working days per month)$\times$(24 hrs per day)/(30 hrs Burn-In cycle)

$N^0(m)$ = number of ovens currently wired with option m.

Decision Variable:

$N(m)$ = number of ovens to be wired with option m.

The model for the wiring plan can be written as

$$\text{Minimize} \sum_m |N(m) - N^0(m)|$$

subject to

$$H \cdot \sum_m N(m) \cdot C(i,m) \geq D(i) \qquad \forall\, i \quad (1)$$

$$\sum_m N(m) = J \qquad (2)$$

$$N(m) \geq 0 \text{ and integer} \qquad \forall\, m \quad (3)$$

The objective function represents the total number of ovens to be re-wired. Constraint (1) ensures that the capacity for each type of PCB is sufficient to satisfy its monthly demand. Constraint (2) states that there are altogether J ovens available and each oven has to be wired with some option.

3.2 The Release Plan

A good release plan should ensure that demands for various sub-assemblies are met and that WIP is minimized throughout the line. Because a large WIP is observed at the burn-in section, it is important to ensure that the daily release corresponds to a mix of sub-assemblies that would be "loadable" into the burn-in oven, once they arrive there. The basic premise underlying this is that the PCBs that are released on day t_1 will indeed all reach the burn-in section on some later day t_2. Although this is not likely to occur exactly, it constitutes a good basis for a release policy. An ideal release plan should therefore (a) satisfy the just described mix criterion, and (b) meet the daily demand.

The order release integer program aims at reconciling these two objectives when necessary, i.e., the release plan will take into consideration the **captives** available for the purpose of burn-in and ensure that the least number of excess PCBs will be released. In case more than the daily demand has to be released in order to meet the minimum limit, even after considering the captive PCBs, the daily demand for the remaining days in the month will be adjusted to reflect the amount over-produced. Over-production may also take place because the number of panels released for some PCB types may contain more than the ideal number of PCBs. In this case the daily demand for this PCB for the remaining days in the

month will be reduced accordingly. Since all rejects in the testing section are repaired and there is practically no scrap, no additional units, over and above this amount are released. The model for determining the release plan is given below:

Indices:

i = index for PCB types.

k = index for Burn-In ovens.

j = index for configurations.

Parameters:

$A(i,j)$ = maximum requirement of PCB i for configuration j.

$B(i,j)$ = minimum requirement of PCB i for configuration j.

$CAP(i)$ = the total number of captive board i available for Burn-In.

$d(i)$ = daily demand for PCB i.

W_r = weight assigned to PCBs. ($W_r = 10$ is used in all our experiments).

W_c = weight assigned to captive boards. ($W_c = 1$ is used in all our experiments).

Decision Variables:

$X(i,k)$ = number of PCB i processed by Oven#k.

$Y(i,k)$ = number of captive board i required by Oven#k.

$$Z(k,j) = \begin{cases} 1 & \text{if oven k uses configuration } j \\ 0 & \text{otherwise.} \end{cases}$$

The model for the release plan can be written as

Minimize $\sum_i \sum_k [W_r \cdot X(i,k) + W_c \cdot Y(i,k)]$

subject to

$$\sum_j B(i,j) \cdot Z(k,j) \leq X(i,k) + Y(i,k) \leq \sum_j A(i,j) \cdot Z(k,j) \quad \forall\, i,\ k \quad (4)$$

$$\sum_j Z(k,j) \leq 1 \quad \forall\, k \quad (5)$$

$$\sum_k Y(i,k) \leq CAP(i) \quad \forall\, i \quad (6)$$

$$\sum_k X(i,k) \geq d(i) \quad \forall\, i \quad (7)$$

$$Z(k,j) \in \{0,1\} \quad \forall\, k,\ j \quad (8)$$

$$X(i,k),\ Y(i,k) \geq 0 \quad \forall\, i,\ k \quad (9)$$

This model minimizes a composite objective function with two terms: the number of real PCBs released, and the number of captive boards; the first term has a higher weight (i.e., 10) than the second (i.e., 1), reflecting the higher priority of releasing as closely as possible to the adjusted daily demand. There are four groups of constraints. The first group (constraint 4) ensures that the quantity of boards (including the captive PCBs) in any oven is between its required minimum and maximum limits as determined by the wiring of that oven and its selected *configuration*. A configuration is defined as the number of OC-12, OC-48, and REGEN to load for a firing of the oven. The second group of constraints (5) assert that each oven may take at most one configuration for that day. If the result of the model indicates zero as the configuration number for an oven, this means that the oven is not used for this release. The third group of constraints (6) ensure that the total number of captive PCBs used for each type does not exceed the quantity available. The fourth group of constraints (7) ensure that the total number of PCBs released of each type is no less than its adjusted daily demand. The adjusted daily demand is computed for each PCB type as the monthly demand minus the quantity released in previous days minus the number of rejects, divided by the remaining number of workdays in the current month.

3.3 The Burn-In Plan

The goal of the burn-in plan is to reduce the waiting time for the sub-assemblies that have already arrived at the burn-in section. The observed wait in the burn-in buffer is large, so that substantial lead time savings may be secured by reducing the WIP there. As explained earlier, because of unequal processing times and the occurrence of random events such as test failures and machine breakdowns, sub-assemblies that are ready for burn-in test at the end of a day may not exactly match the release plan of some previous day. In this case one could either hold off firing the ovens and wait until all the remaining sub-assemblies have been collected, or one may construct a burn-in plan based on how many of each type are currently available, or will soon be available for burn-in. We do not expect the first approach to perform well, since the delay of perhaps a few sub-assemblies would hold up the entire batch and provoke long waiting time before the burn-in test.

Instead, we choose the second approach and construct a burn-in plan that will in general differ from the release plan. The challenge of such a burn-in plan is to balance three goals which often contradict one another. The three goals are (1) to burn the sub-assemblies that are ready and available as soon as possible; (2) to respect the minimum and maximum limits of each burn-in oven; and (3) to wait for sub-assemblies that have yet to arrive in order to minimize *their* waiting time. Overall, our approach tries to maximize oven utilization, a task which is make complicated by the complex nature of the oven loading rules.

The minimum requirements of burn-in ovens prevent the sub-assemblies from being sent for burn-in as soon as they arrive. They have to wait at least for the minimum requirements to be collected. However, prompt firing of any oven with just the minimum requirements may under-utilize the oven capacity and incur long waiting time for the boards that are to come later on. Our burn-in plan attempts to strike a balance between the short term view and the long term view by taking a planning horizon of twenty-four hours when determining the loading of the ovens. Therefore, the decision is not only based on what sub-assemblies are *currently* available but also takes into consideration what sub-assemblies are *likely to become available* in the next sixteen hours. The Automated Insertion, Manual

Insertion and Assembly, and the Testing sections work for two shifts while the Burn-In section operates over three shifts. As can be seen from Table 2, the total processing times of all operations before the burn-in is between 2 and 4 hours. Each oven takes 3 hours for loading, 24 hours for testing, and 3 hours for unloading. At the beginning of each day (i.e., 8:00 am), the burn-in department determines the following: which sub-assemblies are expected to be ready for the burn-in test in the next sixteen hours (i.e., by 12 am) and which ovens and captive boards will become available in the next twenty four hours. Note that the identities of and times at which the ovens will become free are perfectly predictable, whereas the information on the availability of sub-assemblies must be secured via an imperfect estimation procedure, described later. Based on this information, the burn-in plan is created.

The objective of the estimation procedure is to find out at 8:00 am every day how many sub-assemblies of each type are likely to finish the functional and in-circuit tests and become available for the burn-in test within the next sixteen hours. We refer to those sub-assemblies that could be available as 'admissible'. Thus all the sub-assemblies that are currently sitting in the burn-in stock are admissible. We then look at the sub-assemblies that are waiting for the functional and in-circuit tests and see how many of them can also become admissible. This is tantamount to predicting how many sub-assemblies of each type will clear the two tandem queueing systems comprising the in-circuit and the functional tests. The precise estimation procedure used is given in Appendix 1.

The model for the burn-in plan is presented below:

Indices:

i = index for PCB types.

k = index for Burn-In ovens.

j = index for configurations.

Parameters:

K' = the set of ovens to be available during the next twenty-four hours.

$A(i,j)$ = maximum requirement of PCB i for configuration j.

$B(i,j)$ = minimum requirement of PCB i for configuration j.

$E(i)$ = estimated number of PCB i to be available in the next sixteen hours.

$CAP(i)$ = the number of captive board i to be available in the next twenty-four hours.

W_r = weight assigned to PCBs. ($W_r = 30$ is used in all our experiments).

W_c = weight assigned to captive boards. ($W_c = 1$ is used in all our experiments).

Decision Variables:

$X(i,k)$ = quantity of product i processed in Oven#k.

$Y(i,k)$ = number of captive board i required by Oven#k.

$$Z(k,j) = \begin{cases} 1 & \text{if oven k uses configuration } j \\ 0 & \text{otherwise.} \end{cases}$$

The model for the Burn-In plan can be written as

$$\text{Maximize} \sum_i \sum_{k \in K'} [W_r \cdot X(i,k) - W_c \cdot Y(i,k)]$$

subject to

$$\sum_j B(i,j) \cdot Z(k,j) \leq X(i,k) + Y(i,k) \leq \sum_j A(i,j) \cdot Z(k,j) \quad \forall\, i,\ k \in K' \quad (10)$$

$$\sum_j Z(k,j) \leq 1 \quad \forall\, k \in K' \quad (11)$$

$$\sum_k Y(i,k) \leq CAP(i) \quad \forall\, i \in K' \quad (12)$$

$$\sum_k X(i,k) \leq E(i) \quad \forall\, i \quad (13)$$

$$Z(k,j) \in \{0,1\} \quad \forall\, k \in K',\ j \quad (14)$$

$$X(i,k),\ Y(i,k) \geq 0 \quad \forall\, i,\ k \in K' \quad (15)$$

The objective of this program is to maximize the number of PCBs to be Burn-In tested in the next twenty-four hours while using the minimum number of captive boards. The interpretation of constraints (10), (11) and (12) are the same as the first three constrains in

the model for the release plan, except that the ovens and captive boards to be considered are limited to the ones that will be available during the next twenty-fours. Constraint (13) ensures that we only consider those PCBs that are expected to be ready for the Burn-In test. The values of $E(i)$ are determined by the estimation procedure presented in Appendix 1.

3.4 Decisions at Intermediate Stations

The above three plans deal with what appears to be the main operational decisions along the line. There remains however a few secondary decisions to be specified for the simulation program to run unambiguously, as described in the following.

Batching at the wave oven and at in-circuit testing stations

In addition to the setup at the screen printer, setups are also incurred at the wave oven and at in-circuit test stations. Hence the need for a robust batching policy at these two locations. Based on preliminary investigation, the following batching policies were adopted. At the wave oven, each PCB requires one of three different temperature profiles. A setup is needed to switch from one temperature profile to another. In order to minimize the WIP at the wave machine, the profile selected was the one with the largest number of PCBs waiting. This profile remains active till no more PCBs requiring this profile are waiting. At this point a setup is incurred for switching to the profile which has the maximum WIP waiting. At the in-circuit test, a sequence independent setup is incurred for each sub-assembly type. The batch size used is of the same order of magnitude as the release batch size. The justification for this batch size is that it represents the number of sub-assemblies required in a feasible burn-in plan. Since only a small fraction of PCBs go through mold seal operation, we do not batch products here and allow setups to be incurred as the PCB sequence changes.

The queue discipline at the manual insertion stations

The queue discipline at the manual insertion stations is First Come First Served. There are ten different parallel lines of workstations for before wave insertion, while at the after-wave insertion there are twelve parallel workstations. As already mentioned, workers on the parallel lines are cross-trained so that the arriving job may go to the first available line, after waiting in the common queue.

Rules for assembly

After the after-wave insertion, panels are "depaneled" into individual PCBs (if there are multiple PCBs on the panel) and sub-assemblies are generated. There are different procedures for generating sub-assemblies. In some cases, PCBs go to in-circuit test and/or functional test as individual PCBs and assembly is done later, while in other cases, sub-assemblies are generated first and then these are sent for testing. In some cases, testing is done both for the PCB and the sub-assembly. In order to avoid the complexity of including all individual rules in the simulation, the following approximation was used: PCBs requiring depaneling were depaneled after the after-wave insertion and the assembly was done as soon as the entire assembly set was available. In-circuit and functional testing was performed at the level of the sub-assemblies. Wherever necessary, the test times were inflated to reflect test times at both PCB and sub-assembly levels. This rule is conservative in terms of lead times since it forces the generation of sub-assemblies earlier than required.

4 Results and Managerial Implications

We now present experimental results based on the study of the NT Fiberworld production facility and derive insights for the management of lines with batch processing units. We begin with the observation made on the shop floor to the effect that a large portion of the wait occurs in front of those stations which require that logical sets of boards be present, i.e., assembly and burn-in. We observed that these two stations alone account for 65% of

the total wait experienced by the boards.

In order to compare our approach, as presented in section 3, with others, we designed three policies which are given in Table 3. In Policy 1, orders are released based only on the daily demand, i.e., at 8:00 am every day, each assembly's adjusted daily demand is released on to the shop floor in a single batch. The burn-in plan is then applied daily as described in section 3.3. Policy 3 is the dynamic-reactive policy that uses the release plan of section 3.2 for releasing boards and the reactive burn-in plan of section 3.3 for determining, daily, the oven loading. Finally, Policy 2 uses the release plan of section 3.2 both as the release plan and as the burn-in plan. In this policy, the ovens thus wait for the pre-determined mix to arrive before they are fired.

The comparison of Policies 1 and 3 will shed light on the impact of release batch size on lead time since the batches released by Policy 3 are smaller than those by Policy 1. The comparison of Policies 2 and 3 will reveal the impact of a reactive burn-in policy as opposed to rigid planning. Furthermore, for each policy, two different cases are investigated allowing for a high and a low number of captives respectively. For the 'high captive' case we use 500 captive PCBs for each sub-assembly type while for 'low captive' case we use 30 captive PCBs for all sub-assembly types except for one of the sub-assembly types where this number was set to 75. The numbers in the low captive case represent approximately 50% of the maximum number of captives actually utilized on any given day in the case with high captives. Shortage of captive PCBs is therefore sure to occur in the low captive case.

Table 4 contains the main results of our simulation. Each column corresponds to the combination of a policy and a level of captive boards. Each row corresponds to one month. Two initial months were used to "warm-up" the simulation and results obtained for the next eleven months. In each cell, the monthly average lead time is shown (in days) along with the estimated standard deviation (in days). We did not attempt to compute rigorous confidence intervals for the mean lead times of Table 4 due to the excessive computing time this would have required. However, the fact that the overall standard deviations are relatively small and that a large number of boards are processed in a month (typically several thousands) indicates that the error on the monthly lead time average will be very small as compared to

the mean. (Neglecting autocorrelation, one would evaluate a typical value for the error at about 0.01 day for Policy 1 with high captives, a very small number indeed).

Table 5 gives additional information on the average monthly WIP and on the burn-in oven utilization for policy 3 with high captives. It is of course well known that average WIP is proportional to average lead time, due to Little's Law.

Effect of Burn-in Policy: As can be seen from Table 4, the dynamic-reactive approach of Policy 3 outperforms the other two policies for each of the two captive PCB scenarios. Policy 2 consistently performs poorly as compared to the others. This is chiefly due to increased waiting for the released orders to be collected before the burn-in. This situation is aggravated by the fact that due to variability in the line (e.g., breakdowns, poor yield etc.) ovens have to wait longer before a mix can be collected for a burn-in. This is evident when we compare Policy 2 and 3 (with high captives). The wait times up to burn-in are identical for the two policies, but the wait at burn-in under Policy 2 increases considerably (ranging bewteen 80 to 160 hours for different months) as compared to that with policy 3 (which is fairly stable at approximately 18-22 hours for all the months). For Policy 2, the wait at the burn-in represents 80-90% of the total wait time. Our burn-in plan addresses this shortcoming. It reacts to such variations by adjusting the burn-in mix based on the sub-assemblies in the buffer and the expected arrivals. As a result, Policy 3 (with both high and low captives) yields vastly improved lead time and consequently lower WIP over other respective policies.

We also observe that the non-availability of captive PCBs has a much greater impact on the lead times in Policy 2 as opposed to the others. This points towards another advantage of the reactive approach in determining the burn-in mix.

Effect of Release Policy: The role of the release plan can be seen by comparing Policies 1 and 3. The known tradeoff between the increased number of setups versus the reduced waiting time for the collection of batches comes into play here. Policy 3 outperforms Policy 1 by about 0.5 days in terms of lead times indicating the relative importance of reducing waiting times through smaller batches.

It is worth noting that locations where coordination of product mix was required

(e.g., burn-in and assembly) exhibited higher contributions to the lead time. In one example (for Policy 3 with high captives), we observed that 50% and 17% of the wait time were contributed by the burn-in and assembly waits respectively. We have also observed that too many sub-assemblies of the same type queue up at a particular location (e.g., In-Circuit and Functional tests) while stations for other types of products are idle. This contributes to congestion at some stations. Once again, the superiority of the release plan as determined by the model in section 3.2 is obvious. It takes into consideration potential oven loadings in determining order releases, thereby alleviating the above situation. The practice of ignoring batch processors while releasing orders on to the shop floor leads to excessive WIP due to the poor coordination of the mix. Similarly, if we do not control the impact of variability, coordination across the product mix (which is essential for operating batch processors) will deteriorate. (Needless to mention, management's priority should be towards eliminating the sources of variability.) Our dynamic-reactive policy (i.e., Policy 3) takes the above issues into account. In releasing orders, it considers the potential burn-in loading mix but as PCBs/sub-assemblies get affected by variability in the line, it reacts by adjusting the burn-in mix that should be used in oven runs. The robustness of this policy is exhibited by stable lead times (mean and standard deviation) fairly independent of the demand, and relatively consistent levels of capacity utilizations. It can be observed from Table 5 that average lead times and standard deviations change by less than 5% even when the demand is decreased by 60% or increased by 30%.

Effect of Forced Utilization: Another managerial practice that often leads to higher WIP relates to resource utilization. We have observed at several plants (including the current one) a propensity to operate scarce resources at high levels of utilization. Karmarkar (1987a) has shown the perverse effect of utilization of a single machine on congestion. This impact is accentuated in complex multi-station lines and especially those with batch processors. Table 6 shows the impact on leadtime when capacity utilization requirements are imposed on batch processors, i.e., when a burn-in oven is run only when sub-assemblies representing a certain fraction of the capacity of the ovens have been collected. (Note that this "space" utilization is different from "time" utilization. The effect of maximizing the later could also lead to

delays as more runs of the oven may be needed to burn-in the entire demand). It can be seen that high capacity utilization restriction can lead to large lead times. In our case, both the minimum-maximum requirement on sub-assemblies and the capacity utilization restrictions interact to yield poor lead times. This effect is relatively unimportant up to 50% forced minimum utilization of burn-in ovens (in fact we observe that average lead times may be marginally reduced for such a policy). However the performance considerably deteriorates when the minimum restriction is increased to 75% and both the lead times and standard deviations are observed to increase substantially (often in excess of 500%). Moreover, often unbalanced demands for different sub-assembly types can prevent the formation of logical mixes for burn-in for a given utilization level thereby causing excessive delays at the burn-in.

5 Conclusion

In this research, we have developed a fairly robust methodology for managing manufacturing lines with batch processors. Order releases are determined based on product mix requirements of the batch processors while the loading of the batch processors takes into consideration the variability in the manufacturing line. This mechanism dynamically reacts to the state of the shop and the loading patterns of the batch processors. As a guideline, one should first identify the locations where WIP accumulates, determine why WIP tends to accumulate at these locations and then design policies accordingly rather than using general recipies for managing such lines.

The procedure that we have developed is very useful in several respects - apart from being used as a control mechanism for synchronizing production on the shop floor to reduce lead time and WIP, it can be used for resource planning over a planning horizon. Some of the key conclusions could be summarized as follows:

• Considerable reduction in lead times were achieved using our procedure. For our test data, the observed average lead times in the plant were close to 15 days per sub-assembly and the mandate of the project was to reduce them to near 3 days. As can be seen from the results, this objective has been clearly achieved;

- The logical constraints governing the batch processors drive the planning process and should be explicitly considered in order release and loading policies;
- Given the variabilities in the manufacturing line, it is always better to develop a separate reactive burn-in loading plan rather than use a fixed plan;
- The managerial objective of maximixing capacity utilization (i.e., space used in the batch processors) could lead to long lead times as it tends to postpone the firing of the batch processors; and
- The procedure allows one to determine periods where additional capacity would be needed in order to maintain low WIP/lead times.

Though our procedure was developed for a specific production line, the above conclusions and the general approach remain valid for manufacturing lines with complex batch processes.

The solution from the burn-in plan also gives the number of captive PCBs needed for each type per month. This is useful information for purposes of planning, especially since the sunk cost associated with each captive PCB is quite high. Similarly, a manager can make capacity related decisions (i.e., number of shifts, worker levels, additional machine requirements etc.) using lead times in different demand scenarios determined by our model. The varying lead time figures (as well as WIP levels) could also point towards periods (and locations) where extra resources could be added to reduce lead time to desired levels.

Several additional interesting issues arise in the context of this research that should be addressed in the future. A direct extension of this work would be to develop release polices that are dependent on the state of the shop. This would make order releases more reactive.

Appendix 1: Estimation Procedure

The estimation procedure involves the following four steps:

Step 1: Calculation of Expected Processing Times.

The expected processing time, E_i^r, for PCB i (r=F for functional and r=C for in-circuit (I/C) tests) is computed as follows,

$$E_i^r = T_i^r + P_i^r(TS_i^r + RP_i^r + RT_i^r)$$

where T_i^r, P_i^r, TS_i^r, RP_i^r, and RT_i^r represent respectively the test time, probability of failure, trouble shooting time, repair time, and retest time.

Step 2: Estimation of the number of PCBs at the Functional test that will become ready for the Burn-In test within the next sixteen hours.

Denote by $j(f)$ the j^{th} test station at the Functional test location f, $1 \leq f \leq 8$. Step 2 is accomplished by performing a sequence of operations shown below:

(1) Obtain from the simulation model the values of B_i and $i(f,n)$, representing respectively the number of PCB i waiting before the Burn-In ovens and the PCB type of the n^{th} PCB waiting before the Functional test location f, $1 \leq f \leq 8$, $n = 1, 2 \cdots$. (PCBs at this time are waiting in a single queue before their designated functional test location.)

(2) Initialize to zero the queue waiting time, denoted by $Q_{j(f)}^F$, of each functional test station $j(f)$ (in terms of the cumulative processing time of PCBs to be processed).

(3) According to their waiting sequence, PCBs are allocated one by one to a test station with the shortest queue length. Once a PCB is allocated to a test station, (note: there can be multiple test stations at each location) the queue waiting time at that station is updated by adding to it the PCB's expected process time for Functional test. Clearly, the updated queue waiting time represents the expected sojourn time (waiting plus processing) experienced by the PCB before it is ready for the burn-in test.

(4) The allocation process described in (3) for a functional test location stops, either, when

the shortest queue waiting time at any test station is equal to or greater than sixteen hours, or when all the PCBs waiting before that test location have been allocated to a test station.

(5) At the end of the allocation process, let $L(i)$ be the number of type i PCBs whose expected sojourn times are less than or equal to sixteen hours and S be the set of PCB types for which the expected sojourn times at all designated test stations are equal to or greater than sixteen hours. If the set S contains all the PCB types (which means that no more than $L(i)$ for PCB i is expected to complete its Functional test within the next sixteen hours), go to Step 4, otherwise, go to Step 3. In other words, if for some PCB of type i the expected sojourn time of all the units at the Functional Test is less than sixteen hours, then only is there a need to examine the I/C test to check if anymore units of that type could arrive at the Functional test within the specified sixteen hours.

Step 3: Estimation of the number of PCBs at the I/C test that will become ready for the Burn-In test within the next sixteen hours.

Denote by $j(c)$ the j^{th} test station at the I/C test location c, c=1,2. Step 3 is accomplished by performing a sequence of operations shown below:

(1) Obtain from the simulation model the values of $i(c,m)$ and $b(c,m)$, representing respectively, the type and number of PCBs in the m^{th} batch waiting before I/C test location $c = 1,2$; $m = 1,2\cdots$.

(2) Initialize to zero the queue length, denoted by $Q^C_{j(c)}$, of each I/C station $j(c)$ in terms of the cumulative processing times of PCBs to be processed.

(3) According to the waiting sequence of their batch, PCBs in each batch at the I/C test is allocated one by one to the test station with the shortest queue length. The expected sojourn time, $T^C_{(c,m),k}$, of the k^{th} PCB in the m^{th} batch for the I/C test is given by

$$T^C_{(c,m),k} = \min_{j(c)}\{Q^C_{j(c)}\} + k \cdot E^C_{i(c,m)} + ST$$

where $j(c)$ is an I/C test station designated to that PCB type $i(c,m)$, $Q^C_{j(c)}$ is the queue length of the test stations $j(c)$ just before the first PCB in this batch is allocated, and ST is the set-up time when an I/C test station switches from one batch to another.

(4) Once the sojourn time of a PCB for the I/C test is obtained, we immediately compute its expected total sojourn time, $T_{(c,m),k}$, before it becomes ready for the burn-in test. $T_{(c,m),k}$ is given by

$$T_{(c,m),k} = max\{Q^C_{(c,m),k}, \min_{j(f)}\{Q^F_{j(f)}\}\} + E^F_{i(c,m)}$$

where $Q^F_{j(f)}$ is the queue length of its designated functional test station $j(f)$. Notice that the quantity,

$$max\{Q^C_{(c,m),k}, \min_{j(f)}\{Q^F_{j(f)}\}\},$$

is the point in time when a functional test station first becomes free after the PCB's expected completion time for the I/C test. If $T_{(c,m),k}$ is greater than sixteen hours, the PCB type $i(c,m)$ is added to set S, otherwise, $L(i(c,m)) = L(i(c,m)) + 1$.

(5) The queue length, $Q^F_{j(F)}$, of the functional test station $j(f)$,

$$j(f) = arg\min_{j(f)}\{Q^F_{j(f)}\}$$

is immediately updated by

$$Q^F_{j(f)} = Q^F_{j(f)} + max\{0, Q^C_{(c,m),k} - Q^F_{j(f)}\} + E^F_{i(c,m)}$$

(6) The queue length of the I/C test station, however, is not updated until the expected total sojourn times for all the PCBs in the batch are computed. Once the full batch is allocated to a test station $j(c)$, the queue length of that test station is updated as follows

$$Q^C_{j(c)} = Q^C_{j(c)} + b(c,m) \cdot E^C_{i(c,m)} + ST$$

(7) Step 3 continues until either PCBs in all the batches waiting at the I/C test have been allocated to a test station, or the set S contains all the PCB types.

Step 4: Computation of the total expected number of PCBs that will become ready for the Burn-In test within the next sixteen hours

This number, denoted by $E(i)$ for PCB type i, is given by

$$E(i) = B(i) + L(i)$$

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Transmission Devices	Subassemblies	PCBs
OC-12	7E02XX	7E0210
		7E0208
		⋮
	7E08XX	7E08AA
	⋮	
OC-48	8E01XX	8E0142
		8E0134
		⋮
	7E08XX	7E08AA
	⋮	
REGEN	8E03XX	8E0302
		8E0134
		⋮

Table 1: The Product Structure

Work Stations	Processing Times (in minutes)	Setup Times (in minutes)
Screen Printer	0.3	10.0
Surface Mount (top side)	3.0 - 4.01	
Auto Insertion	1.5 - 2.0	
Surface Mount (bottom side)	1.0 - 1.1	
Connector Assembly	4.0 - 5.0	
Mold Seal	1.0 - 1.2 (+1 hr. Drying)	1.0
Modification Before Wave	5.0 - 30.0	
Before Wave Insertion	2.0 - 33.0	
Wave Soldering	5.0	1.0
After Wave Insertion	20.0 - 30.0	
Assembly	0.5	
In-Circuit Test:		
Test	2.0 - 6.0	5.0
Trouble Shooting	5.0 - 15.0	
Repair	15.0 - 20.0	
Functional Test:		
Test	10.0 - 60.0	
Trouble Shooting	20.0 - 30.0	
Repair	15.0 - 30.0	
Mechanical Assembly	15.0 - 30.0	
Burn-in	30 hours	

Table 2: Processing and Setup Times

Policy 1: Release Plan=Daily Demand Burn-in Plan=Results of the Burn-in Plan Model
Policy 2: Release Plan=Results of the Release Plan Model Burn-in Plan=Release Plan
Policy 3: Release Plan=Results of the Release Plan Model Burn-in Plan=Results of the Burn-in Plan Model

Table 3: Shop Synchronization Policies

Month	Mean (Standard Deviation) of Production Lead Times (in days)					
	Policy 1		Policy 2		Policy 3	
	High Captive	Low Captive	High Captive	Low Captive	High Captive	Low Captive
1	3.32	3.86	5.82	8.65	2.84	3.54
	(0.61)	(1.31)	(2.22)	(2.84)	(0.52)	(1.26)
2	3.24	3.97	6.64	10.83	2.80	3.51
	(0.58)	(1.48)	(2.28)	(2.80)	(0.48)	(1.59)
3	3.16	3.71	10.04	16.26	2.91	3.60
	(0.60)	(1.34)	(3.26)	(2.91)	(0.53)	(1.82)
4	3.27	3.57	10.96	23.29	2.83	3.48
	(0.59)	(0.83)	(4.55)	(2.83)	(0.50)	(1.36)
5	3.17	3.41	10.26	28.67	2.76	3.63
	(0.58)	(0.72)	(4.37)	(2.76)	(0.50)	(1.20)
6	3.19	3.34	8.87	33.67	2.88	3.15
	(0.60)	(0.66)	(5.33)	(2.88)	(0.53)	(0.94)
7	3.02	3.13	11.66	37.28	2.88	3.27
	(0.68)	(0.74)	(7.10)	(2.88)	(0.61)	(1.09)
8	3.26	3.37	5.86	41.94	2.87	3.00
	(0.65)	(0.71)	(4.12)	(2.87)	(0.56)	(0.64)
9	3.31	3.93	7.10	31.35	3.03	3.44
	(0.64)	(1.28)	(3.14)	(3.03)	(0.64)	(1.05)
10	3.24	4.77	8.50	30.98	3.02	4.33
	(0.68)	(3.13)	(4.55)	(3.02)	(0.64)	(2.71)
11	3.17	4.85	7.41	36.29	2.89	4.38
	(0.60)	(3.64)	(5.79)	(2.89)	(0.58)	(3.30)

Table 4: Mean and Standard Deviation of Production Lead times

Month	# of Boards Processed	Mean Lead Time	Standard Deviation of Lead Time	Average WIP	Utilization of Ovens
1	4657	2.84	0.52	606.81	33.03 %
2	4436	2.80	0.48	555.64	30.60 %
3	3603	2.91	0.53	478.65	25.48 %
4	4385	2.83	0.50	557.90	30.22 %
5	3940	2.76	0.50	488.28	27.77 %
6	4039	2.88	0.53	532.74	28.17 %
7	1684	2.88	0.61	202.80	11.29 %
8	3817	2.87	0.56	541.86	27.40 %
9	5130	3.03	0.64	696.80	35.75 %
10	4392	3.02	0.64	590.59	30.37 %
11	4381	2.89	0.58	588.80	31.75 %

Table 5: Detailed Simulation Results using Policy 3 and High Captive

Month	Mean and Sdandard Deviation of Production Lead Times		
	75 % Restriction	50 % Restriction	No restriction
1	6.70 (6.11)	2.80 (0.54)	2.84 (0.52)
2	7.76 (8.09)	2.80 (0.50)	2.80 (0.48)
3	9.59 (11.39)	2.88 (0.61)	2.91 (0.53)
4	11.68 (14.94)	2.85 (0.53)	2.83 (0.50)
5	13.05 (16.84)	2.98 (0.61)	2.76 (0.50)
6	14.51 (19.87)	2.84 (0.58)	2.88 (0.53)
7	19.38 (28.51)	3.69 (6.97)	2.88 (0.61)
8	21.48 (30.68)	2.93 (0.76)	2.87 (0.56)
9	21.62 (31.37)	3.19 (0.92)	3.03 (0.64)
10	21.58 (31.31)	3.85 (1.90)	3.02 (0.64)
11	21.93 (31.59)	3.16 (1.36)	2.89 (5.79)

Table 6: Mean and Standard Deviation of Production Lead Times with Oven Loading Restrictions using Plolicy 3 and High Captive

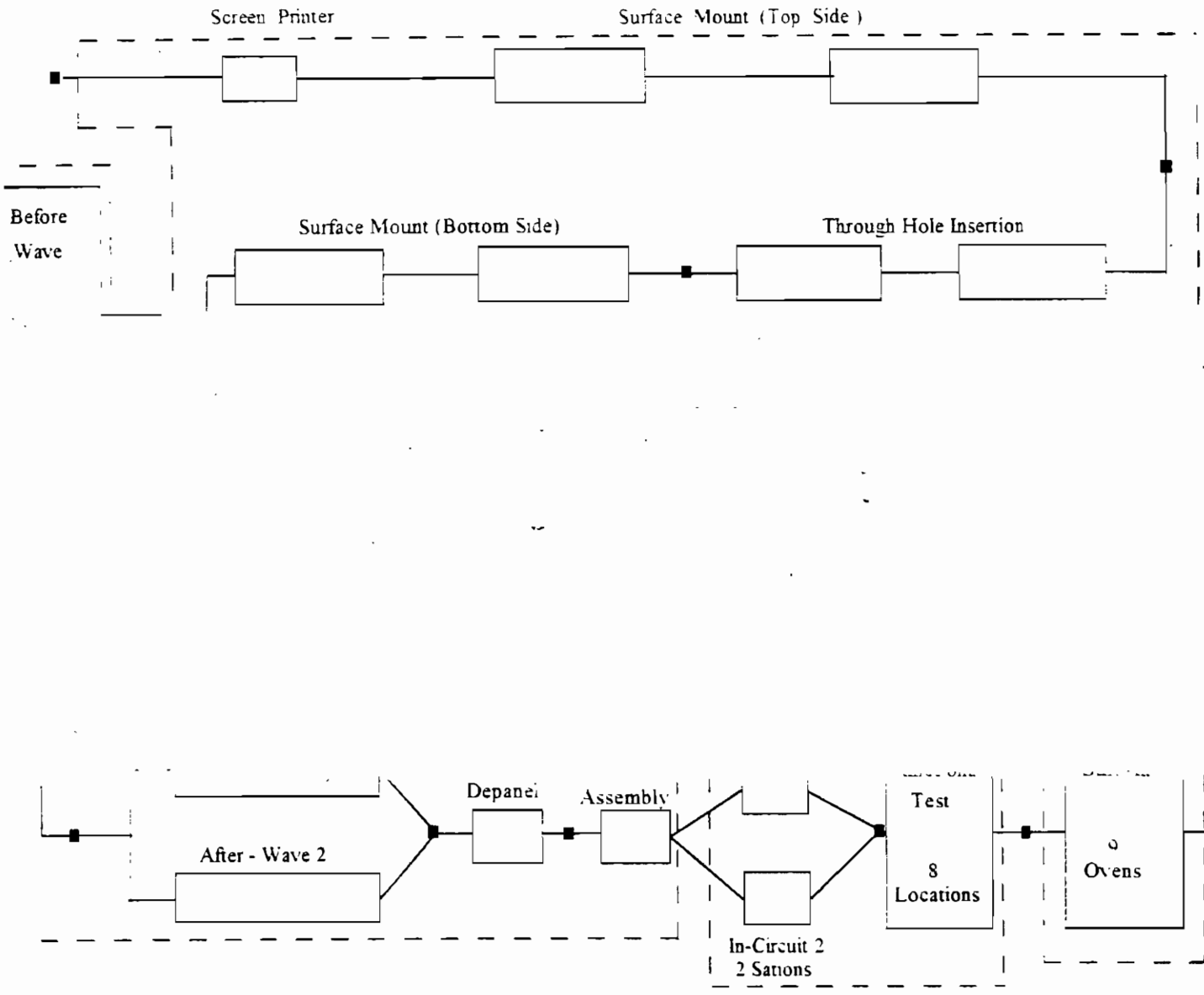

Figure 1. Representation of the Transmission Device Manufacturing Line

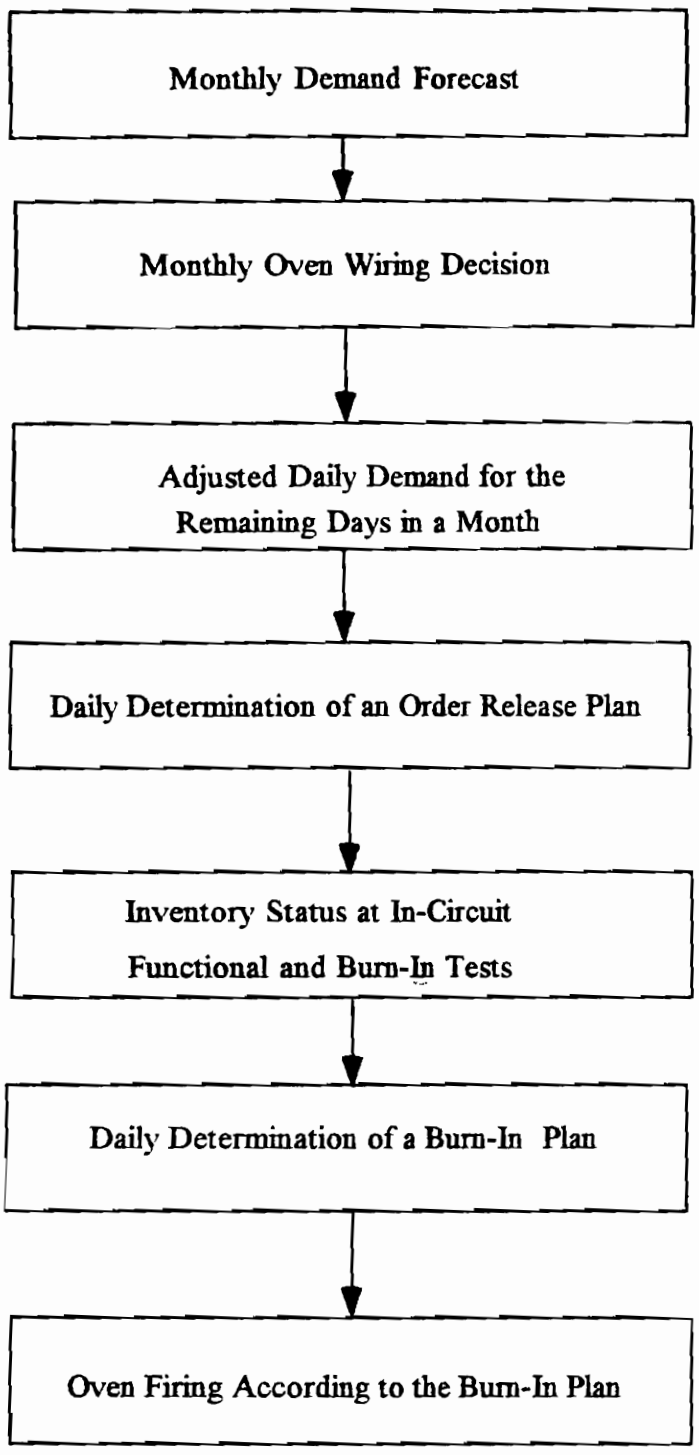

Figure 2: Decision Sequence

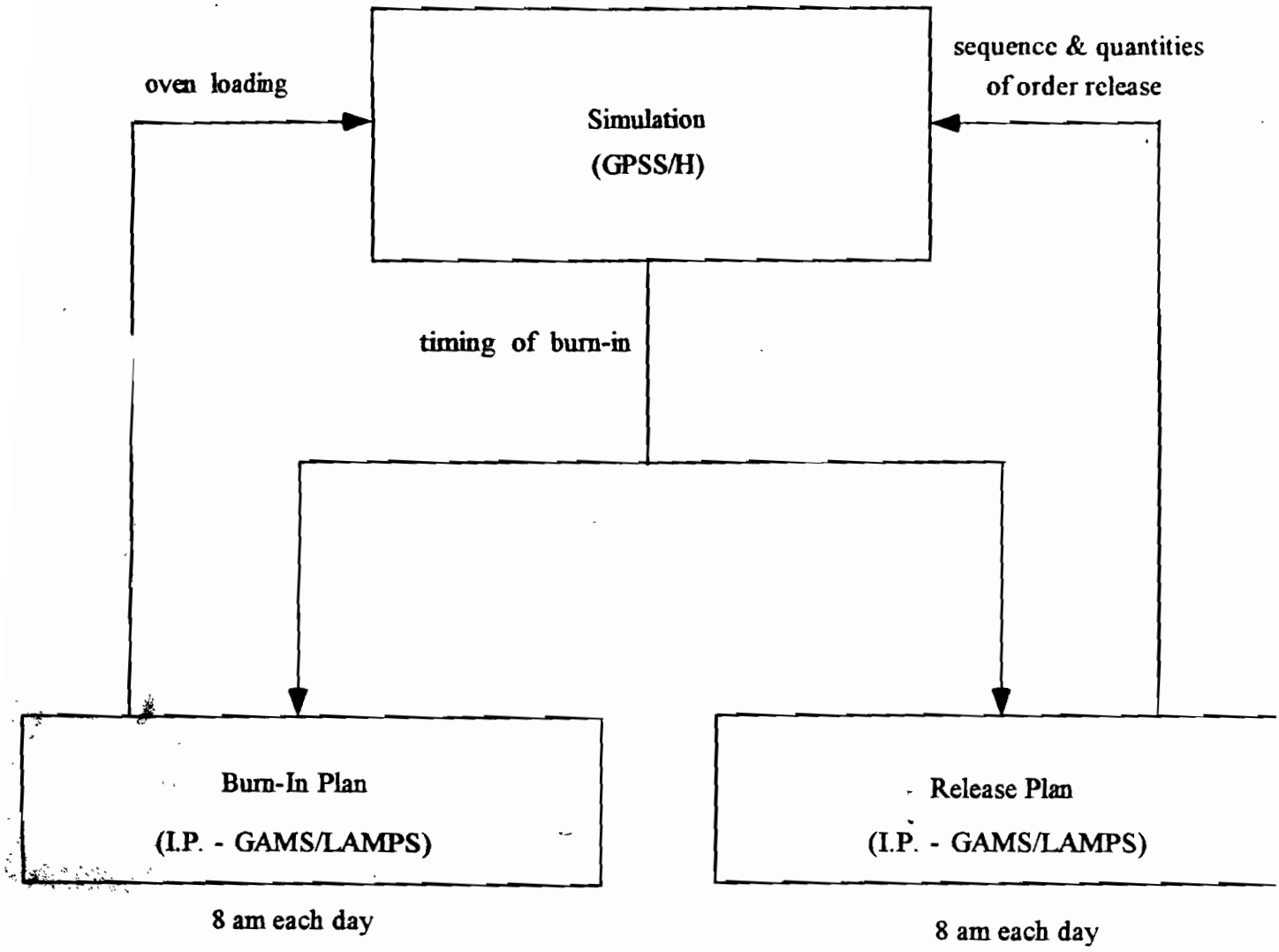

Figure 3: Planning Methodology